New Debug Cable for Cortex-M Series

From spring 2007, Lauterbach will be delivering a new version of the Cortex-M family debug cable. The most important innovation is that the debug cable not only supports standard JTAG but also the 2-pin debugging interfaces, cJTAG and SW-DP.

cJTAG

cJTAG (IEEE P1149.7) is an on-chip debugging interface defined by MIPI Alliance Inc. As an alternative to the 5-pin standard JTAG interface, a 2-pin interface has been defined consisting of a clock line and a bidirectional data line (see Fig. 1).

Serial Wire Debug Port (SW-DP)

In the case of SoCs (system on chip) where the debugging and trace functionality is based on CoreSight technology, the external debugger no longer communicates directly with the TAP controllers of the individual cores but via a so-called Debug Access Port (DAP). The task of the DAP is to distribute the debugging commands to the individual cores. Depending on the implementation of on-chip debugging in the individual core, communication takes place as follows:

- Cores with a memory mapped debug register are controlled with the help of bus accesses. Cortex-M, for example, works with this mechanism.

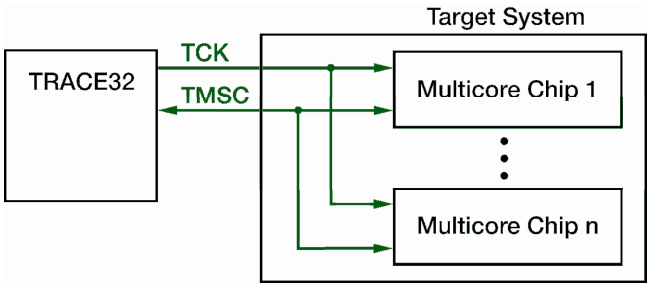

Fig. 1 The cJTAG interface, here for multichip target hardware

- Cores that work with a traditional TAP controller for debugging are still controlled using JTAG sequences.

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Either standard JTAG or the 2-pin-wide Serial Wire Debug Port specified by ARM is used as the interface between the debugger and the DAP (see Fig. 2). To achieve fast download rates for the 2-pin debugging interfaces, the on-chip debugging interface works with frequencies of up to 100 MHz. To exclude reflections by the debugging cable at high frequencies, the termination of the debugging signals has been moved to the target hardware connector.

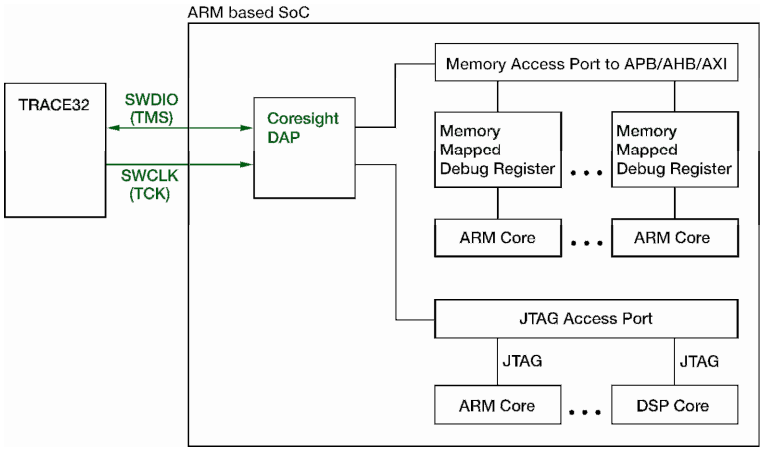

Fig. 2 The Serial Wire Debug Port as a 2-pin interface between the debugger and the DAP

Andrea Martin, February 2007