

TRACE32®

DEBUG & TRACE

TriCore™ AURIX™



A photograph of a car's side mirror. The mirror reflects a blurred scene of a city street at night with lights from cars and buildings. Overlaid on the image is a large amount of C++ code, which appears to be part of a driver or application for a TriCore processor. The code includes functions like `TC4_mix`, `CLS_classify`, and `core0_main`, dealing with buffers, processing, and classification. The background is dark, making the bright reflections and the white text of the code stand out.

TriCore™

TriCore™ AURIX™ at a glance

For more than 20 years Lauterbach has been supporting the latest TriCore™ AUDO™ and AURIX™ microcontrollers. Our tool-chain offers:

- Debugging of all TriCore CPUs and auxiliary cores.
- Tracing of TriCore CPUs and some auxiliary cores via on-chip trace, high-speed serial trace or DAP streaming.
- Code Coverage according to ISO 26262 (Tool Qualification Support Kit)
- AUTOSAR-aware debugging & profiling



TriCore™ AURIX™

TriCore™ AURIX™ Debug Solutions



Single debug solution for all cores		
target system	core type	core state
1: Chip		
1: SMP Sub System	TriCore	stopped
0: TriCore0	TriCore	stopped
1: TriCore1	TriCore	stopped
2: TriCore2	TriCore	stopped
3: TriCore3	TriCore	stopped
4: TriCore4	TriCore	stopped
5: TriCore5	TriCore	stopped
2: Core	HSM\ARM	stopped
3: SMP Sub System	GTM	
0: Core	GTM	stopped
1: Core	GTM	stopped
2: Core	GTM	stopped
3: Core	GTM	stopped
4: Core	GTM	stopped
5: Core	GTM	stopped
6: Core	GTM	stopped
7: Core	GTM	stopped
4: TC3X_SCR	i8051	running

TRACE32® enables concurrent debugging of all TriCore™ CPUs as well as all auxiliary cores of an AURIX™ SoC.

This allows to examine their interaction in depth.

The above includes:

- TC4xx: up to 6 TriCore™ CPUs, CSR (TriCore™), SCR (XC800), PPU (ARC), GTM
- TC2xx/3xx: up to 6 TriCore™ CPUs, HSM (Cortex®-M), SCR (XC800), GTM

Besides standard features like Step/Go/Break and flash programming TRACE32® offers:

- AUTOSAR-aware debugging
- Debugging of multi-OS configurations
- Hypervisor-aware debugging for Memory Protection Unit (MPU) hypervisors

TriCore™ AURIX™ Trace Solutions

- Records information, generated by the MCDS module, about instruction execution and data accesses of multiple TriCore™ CPUs, GTM and PPU as well as transfers on the on-chip buses and peripheral states transitions.
- Provides triggers and filters to limit recorded data and to use trace buffers effectively.
- Enables long-term recording by streaming trace data to the host (TRACE32® trace streaming).

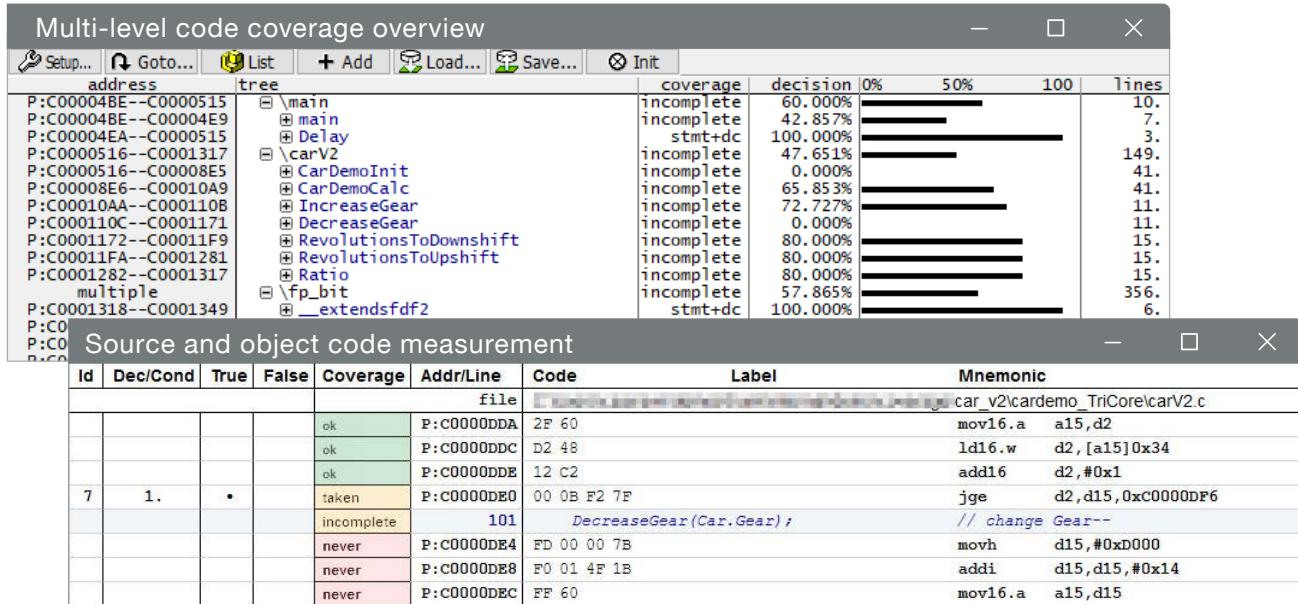
Multicore Trace							
Setup...	Config...	Goto...	Find...	Chart	Profile	MIPS	More
record	run	address	cycle	data	symbol	ti.back	busmaster
		/* Enabling core3 : tc3... */					
		void TCO_StartCore3()					
		{					
		extern void __noinline__ __noreturn__ __jump__ _start_tc3(void);					
		CPU3_PC.U = (unsigned int)_start_tc3;					
		movh.a a15,#0xF888					
		st.w [a15]-0x1F8,d15					
+00004136	50		D:F87FE08	wr-data	70101348	0.080us	
+00004148			P:70100EA6	ptrace	.._intmem\cstart_tc1_start+0x86	2.080us	
+00004154		1	isync				
+00004154		1	st16.w	[a15],d15		0.000us	
+00004154		1	D:F0036258	wr-data	FFFC00F3		
+00004166		1	ld16.w	d15,[a15]			CPU0 DMI
+00004175		1	D:F00362A8	rd-spb	FFFC000F	0.000us	
+00004175		1	D:F0036258	rd-data	FFFC000F		
+00004175		1	movh.a	a15,#0x0			

(feature availability depends on used device)

TriCore™

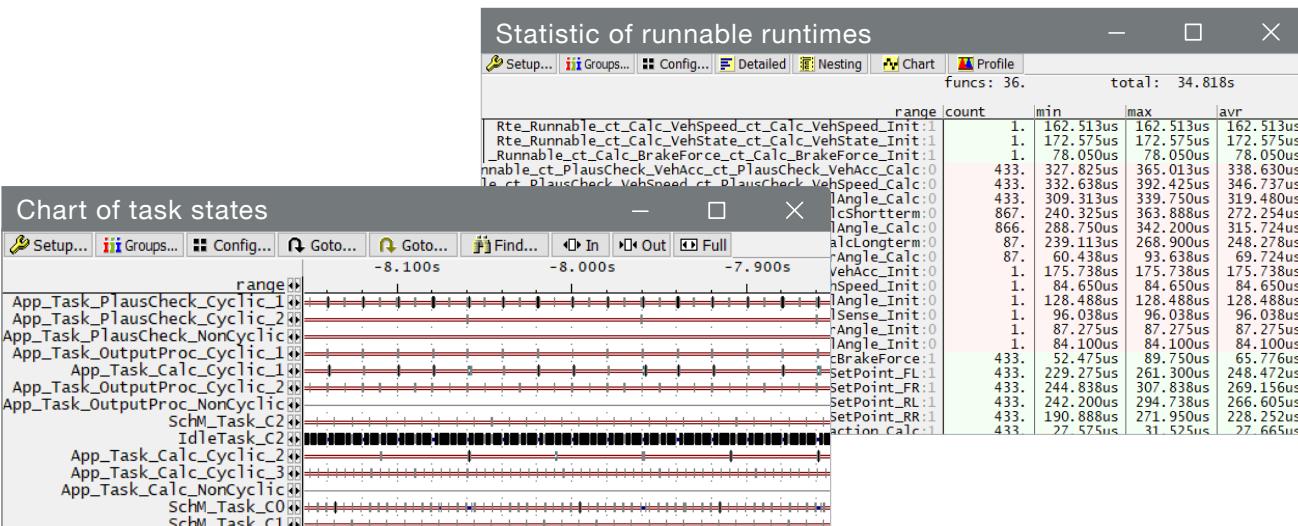
Code Coverage for Functional Safety

- The code coverage functionality supports all metrics required for ISO26262 and other safety standards: statement, branch, MC/DC, function and call coverage.
 - The TRACE32® Tool Qualification Support-Kit streamlines TRACE32® tool qualification effort and costs for the TRACE32® Instruction Set Simulator and all TriCore™ trace solutions.



Profiling for AUTOSAR Classic Platform

- The support for the ARTI standard provides profiling of task state changes, runnables, and interrupts including their state changes. An export to the standardized ARTI format allows data exchange with 3rd-party timing tools.
 - The support for the ORTI standard provides profiling of running tasks and (interrupt) service routines as well as a proprietary export.
 - These use cases are supported by all TRACE32® trace solutions.



Debugger and Trace for TriCore™ AURIX™

POWER DEBUG

DEBUGGER VIA JTAG/DAP

Full-featured AUTO26 connector including watchdog control and arbitration lines for third-party tools. Converters for ECU14 and OCDS16 available.



POWER DEBUG ADD-ON

ON-CHIP TRACE

An additional license enables MCDS trace via on-chip trace memory.



COMBIPROBE 2

DAP STREAMING

Streaming of on-chip trace via DAP debug port to external trace memory (max. 512 MB, max. 30 MB/s). Supports TRACE32® trace streaming.



POWER TRACE

AURORA GIGABIT TRACE

Max. 8 GB of external trace memory, max. 12,5 GBit/s bandwidth per lane. Supports TRACE32® trace streaming.



Software-Only Products

XCP

DEBUG AND TRACE

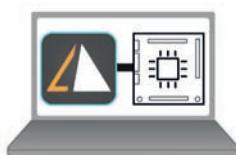
Debugging via XCP Slave supporting "Software Debugging over XCP" standard (ASAM MCD-1 XCP) or ETAS-specific protocol Trace via Onchip trace.



FRONT-END

DEBUG AND TRACE OF SYNOPSYS VDK

Debugging and tracing using TRACE32® on software models before a first hardware prototype is available.



FOR MORE INFORMATION VISIT: www.lauterbach.com/1660

lauterbach.com

Lauterbach GmbH

Altlaufstraße 40

85635 Höhenkirchen-Siegertsbrunn

Telefon: +49 8102 9876-0