Multicore Debug & Trace
The Lauterbach Debugger for RH850 provides high-speed access to the target processor via the JTAG/LPD4/LPD1 interface. Debugging features range from simple step/go/break up to multicore debugging.

Customers value the performance of the flash programming and the intuitive access to all of the peripheral modules.

**Debugging of Complex Chips**

<table>
<thead>
<tr>
<th>Target System</th>
<th>core type</th>
<th>core state</th>
</tr>
</thead>
<tbody>
<tr>
<td>1: R/F701325</td>
<td>V850/RH850</td>
<td>running</td>
</tr>
<tr>
<td>2: Core</td>
<td>V850/RH850</td>
<td>running</td>
</tr>
<tr>
<td>3: Core</td>
<td>V850/RH850</td>
<td>stopped</td>
</tr>
<tr>
<td>0: SMP Sub Sy</td>
<td>GTM</td>
<td>running (idle)</td>
</tr>
<tr>
<td>1: Core</td>
<td>GTM</td>
<td>running (idle)</td>
</tr>
<tr>
<td>2: Core</td>
<td>GTM</td>
<td>running (idle)</td>
</tr>
<tr>
<td>3: Core</td>
<td>GTM</td>
<td>running (idle)</td>
</tr>
<tr>
<td>4: Core</td>
<td>GTM</td>
<td>running (idle)</td>
</tr>
<tr>
<td>5: Core</td>
<td>GTM</td>
<td>running (idle)</td>
</tr>
<tr>
<td>6: SMP Sub Sy</td>
<td>GTM</td>
<td>running (idle)</td>
</tr>
<tr>
<td>7: SMP Sub Sy</td>
<td>GTM</td>
<td>running (idle)</td>
</tr>
</tbody>
</table>

TRACE32 allows concurrent debugging of all RH850 cores.

- The cores can be started and stopped synchronously.
- The state of all cores can be displayed side by side.
- All cores can be controlled by a single script.

TRACE32 provides the option to work in a common environment for all of the RH850 cores and the auxiliary controllers. You can see and analyze the detail of the interaction between the cores and controllers.
Nexus Trace Solutions for RH850

All RH850 emulation devices include a Nexus trace module, which enables multicore tracing of program flow and data transactions. Depending on the device, trace data is routed to one of the following destinations:

- An onchip trace buffer (typically 32KB).
- An off-chip parallel Nexus port for program flow and data tracing.
- A high bandwidth off-chip Aurora Nexus port for extensive data tracing.

The off-chip trace solutions can store up to 4GB of trace data and also provide the ability to stream the data to the host for long-term tracing, thus enabling effortless performance profiling and qualification (e.g. code coverage).

Support for Auxiliary Cores

Debugging and tracing of auxiliary cores is included:

- ICU-M Hardware Security Module
- GTM Peripheral Timer Module

Trace-based Code Coverage

Timing Chart

GTM Debugging

GTM Tracing
Multicore Debugger and Trace for RH850

**Power Debug**

**Debugger for RH850**
Supports JTAG, LPD4, LPD1 modes and serial flash programming mode.
SFT Trace support for instrumented code.

**Onchip Trace Option**
For devices with onchip trace, an additional license is required.

**Power Trace**

**Parallel Nexus Trace**
Trace port data rate up to 100 MHz DDR, enabled through AutoFocus technology.

**Aurora Nexus Trace**
Up to 4 lanes with max. 6.25 GBit/s per lane, reference clock up to 3.125 GHz.

**Front-End**

**Debugger for Synopsys Virtualizer**
It allows debugging software designs before the first hardware prototype is available.

For more information visit: www.lauterbach.com/1701