Höhenkirchen-Siegertsbrunn
Oct 24th, 2017

Lauterbach and SiFive Bring TRACE32 Support for High-Performance RISC-V Cores

World-class microprocessor development tools now available for industry's leading RISC-V IP

Höhenkirchen-Siegertsbrunn, Germany, and San Mateo, Calif. – Lauterbach, the leading manufacturer of microprocessor development tools, and SiFive, the first fabless provider of customized, open-source-enabled semiconductors, today announced the availability of Lauterbach's TRACE32 toolset to provide debug capabilities for SiFive's E31 and E51 RISC-V Core IP, based on the free and open RISC-V ISA. Lauterbach support for SiFive cores is the latest addition to the growing ecosystem of industry-leading development tools to become available for RISC-V based silicon.

Founded by the inventors of RISC-V, SiFive IP addresses the need to combat the rapidly increasing cost of designing and manufacturing new chip architectures, and fulfills the company's mission of democratizing access to custom silicon. Since its launch, SiFive IP has become the de facto leader for RISC-V cores, with more public customers and working silicon in the market than any other RISC-V vendor.

"The addition of Lauterbach's TRACE32 toolset to the SiFive arsenal is a milestone in the continued development of the RISC-V ecosystem," said Yunsup Lee, co-founder and chief technology officer, SiFive. "We have worked closely with Lauterbach to ensure that its TRACE32 toolset provides the highest level of support for the RISC-V debug specification. We look forward to our continued collaboration with Lauterbach to bring additional world-class tools for developers working with SiFive IP."

Lauterbach TRACE32 provides multicore debugging on individual hardware threads of SiFive cores, enabling debugging right from the reset vector, which analyzes startup codes and other key functions. Lauterbach also provides high-level and assembler debugging for a variety of standard ISA extensions, such as compressed instructions and floating point. It also fully supports the JTAG Debug Transport Module (DTM) in all SiFive chips, and has planned support for other debug interfaces such as USB.

"We've seen a growing interest in RISC-V across the industry, and we are pleased to extend our leading toolset to this segment of the market," said Stephan Lauterbach, general manager of Lauterbach. "The availability of TRACE32 debugging tools will help build on the initial success of RISC-V and continue its adoption in a wide array of deployments."

Said Rick O'Connor, chairman of the RISC-V Foundation: "The addition of Lauterbach's world-class solutions to the RISC-V toolset is a testament to the market potential of this new approach to silicon design. Continued collaboration between SiFive and Lauterbach will ensure seamless interoperability between RISC-V hardware and TRACE32."

More information about Lauterbach's TRACE32 can be found here.

For more information on SiFive's Core IP, click here.

Lauterbach GmbH • Altlaufstraße 40 • D-85635 Höhenkirchen-Sieg. • Tel. +49 8102 9876-0 • marketing@lauterbach.com • www.lauterbach.com

About Lauterbach

Lauterbach is the leading manufacturer of complete, modular and upgradeable microprocessor development tools worldwide with experience in the field of embedded designs since 1979. It is an international, well-established company with blue chip customers in every corner of the globe and has a close working relationship with all semiconductor manufacturers. At the headquarters in Höhenkirchen, near Munich, the engineering team develops and produces highly proficient and specialized Development Tools, which are utilized all over the world under the brand TRACE32®. Our branch offices exist in the United Kingdom, Italy, France, Tunisia, on the east and west coasts of the United States, Japan and China. Highly qualified sales and support engineers are also available in many other countries. For more information visit www.lauterbach.com.

About SiFive

SiFive is the first fabless provider of customized semiconductors based on the free and open RISC-V instruction set architecture. Founded by RISC-V inventors Andrew Waterman, Yunsup Lee and Krste Asanovic, SiFive democratizes access to custom silicon by helping system designers reduce time-to-market and realize cost savings with customized RISC-V based semiconductors. SiFive is located in Silicon Valley and has venture backing from Sutter Hill Ventures, Spark Capital and Osage University Partners. For more information, visit www.sifive.com.

MEDIA CONTACTS

Norbert Weiss
International Sales Manager at Lauterbach
+49 (8102) 9876-183
norbert.weiss@lauterbach.com

Jack Kang
SiFive
+1 (510) 673-1309
jack@sifive.com

Leslie Clavin
SHIFT Communications for SiFive
+1 (415) 591-8440
lclavin@shiftcomm.com